REMARKS

Claims 1-33 were originally presented for examination. New claims 34-47 have been added by way of the present response.

Of the claims 1-47 currently pending, claims 1, 16, 25, 34, and 41 are in independent form.

Claims 5-7, 18-20, and 25-33 have been amended. No new matter is introduced hereby.

Support for the claim amendments of the present response may be found in the original specification, for example, at Paragraphs [0024] through [0032], *inter alia*; see also description relating to FIGURE 6 of the present patent application.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding Amendments to the Specification

In the present Office Action, the disclosure is objected to because of certain informalities in Paragraph [0001]. Accordingly, Paragraph [0001] of the original specification has been appropriately amended to include the missing application number and filing date of the co-pending patent application identified therein.

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Regarding Claim Objections - Informalities

Claims 7, 20, and 29 are objected to in the pending Office Action because of certain informalities. Applicant has appropriately amended these claims in response. Accordingly, it is believed that these claim objections have been overcome hereby.

Regarding Allowable Subject Matter

In the pending Office Action, claims 12-15 "are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims."

Applicant gratefully appreciates the identification of allowable subject matter in the pending Office Action. Applicant has added new claims, claims 34-47, wherein the base claims 34 and 41 recite the subject matter that the Examiner has identified as being allowable. Accordingly, it is believed that the new claims 34-47 are in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. §101

In the pending Office Action, claims 25-33 are rejected under 35 U.S.C. §101 because "the claimed invention is directed to non-statutory subject matter. The claimed memory compiler is directed

to computer code not implemented in a computer, or not on computer readable medium."

Applicant has appropriately amended claims 25-33 by way of the present response. It is therefore believed that the pending §101 rejections have been overcome or otherwise rendered moot and claims 25-33 are in condition for allowance.

Regarding the Claim Rejections - 35 U.S.C. §112

Claims 7, 20, and 29 are rejected in the pending Office Action under 35 U.S.C. §112, First Paragraph, as "failing to comply with the enablement requirement." Applicant respectfully submits that these rejections have been overcome or otherwise rendered moot by way of the present response wherein claims 7, 20, and 29 have been amended appropriately.

Regarding the Claim Rejections - 35 U.S.C. §102(e)

Claims 1-6, 8-11, 16-19, and 21-24 are rejected in the pending Office Action under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,691,264 to Huang (hereinafter the *Huang* reference). In connection with these rejections, the Examiner commented as follows with respect to the base claims 1 and 16:

> Regarding claims 1 and 16, Huang Discloses a method and apparatus (Fig. 3) for testing a memory instance (30), comprising:
>
> - scanning test information into a test and repair wrapper (42) integrated with said memory instance (Abstract, lines 1-3);
>
> - providing a strobe control signal (BISR Control, Fig. 5) to said test and repair wrapper for signaling commencement of testing operations with respect to said memory instance (Fig. 5);
>
> - generating, by said test and repair wrapper, at least one of an address signal, a data signal and a command signal based on said scanned test information (address and control signals from 42, Fig. 3);
>
> - executing at least one test with respect to said memory instance responsive to said address, data and command signals generated in said test and repair wrapper (Fig. 3).

Applicant respectfully traverses the foregoing §102(e) rejections and offers the following discussion as support. As defined by the base claim 1, an embodiment of the present invention is directed to a method of testing a memory instance which involves, *inter alia*, scanning test information into a test and repair wrapper integrated with the memory instance. Responsive to providing a strobe control signal, the test and repair wrapper generates at least one of an address signal, a data signal and a command signal based on the scanned test information. Thereafter, responsive to the address, data and command signals generated by

the test and repair wrapper, at least one test is executed with respect to the memory instance.

Similarly, the base claim 16 is directed to an apparatus for testing a memory instance, the apparatus comprising, *inter alia*, a built-in self-test and repair (BISTR) processor associated with the memory instance for scanning test information into a test and repair wrapper integrated with the memory instance, wherein the test and repair wrapper is operable to commence testing responsive to a strobe control provided by the BISTR processor. Also, logic circuitry associated with the test and repair wrapper is operable for generating at least one of an address signal, a data signal and a command signal based on the scanned test information, wherein at least one test may be executed with respect to the memory instance based on the address, data and command signals.

The *Huang* reference is directed to "a method for built-in self-repair of semiconductor memory devices in which the BISR mechanism is substantially independent of the BIST mechanism such that changes to the BIST could be accommodated with little or no modification to the BISR." See column 2, lines 50-55. Thus, as shown in FIGURE 3 of the *Huang* reference, one or more separate BIST units 36, 38, 40 are provided independent of the BISR wrapper 42 with respect to the memory 30. To the extent the present Office

Action attempts to identify the BISR wrapper 42 with the test and repair wrapper recited in the base claims 1 and 16 of the instant patent application, Applicant respectfully submits that it would be a mischaracterization to make such an identification because, at a minimum, there is no scanning of test information into the BISR wrapper 42 of the *Huang* reference. Furthermore, the BISR wrapper 42 does not generate address signals, data signals, and command signals based on the scanned in test information, which signals are used for testing the memory instance as claimed by Applicant. In contrast, the BISR wrapper 42 uses only BIST_DONE and BIST_ERRN error flags from the BIST units 36, 38, 40 in order to effectuate a generic interface between the BISR and BIST units. See column 8, lines 20-35; see also FIGURE 3 of the *Huang* reference. Applicant submits that the BIST_DONE and BIST_ERRN error flags are generated by the BIST units upon completion a test (i.e., the signals are merely post-test flags, not the test information to be scanned into a test and repair wrapper as claimed by Applicant). At column 7, lines 28-39, the *Huang* reference provides that:

> Each BIST receives an ENABLE signal from the BIST/BISR Control Unit 48, and generates an error flag when a defect is detected (ERRN) and a flag indicating that the test stage is complete (BIST_DONE). Since BISTs 36, 38 and 40 each test different portions of the memory, their flags are combined by the BISR 42. The BISR uses the flags, together with the current memory address, to perform self-repair of the accessible memory. Overall

> status and results are presented by the BISR 42 as externally accessible signals ERRN, FAIL and DONE flags 44. Operation of the three BISTs and the BISR is coordinated by the BIST/BISR Control Unit 48.

In other words, the BISR wrapper 42 of the *Huang* reference does not perform the tests, rather only self-repair. Since the BISR wrapper 42 does not perform any tests, it does not generate the necessary address/data/command signals based on scanned in test information for purposes of executing a test with respect to the memory as claimed by Applicant. Accordingly, it would be incorrect to equate the BISR wrapper 42 of the *Huang* reference with the claimed test and repair wrapper, into which test information is scanned, and which generates appropriate address/data/command signals for performing tests.

Based on the foregoing, Applicant respectfully submits that the base claims 1 and 16 are not anticipated or suggested by the applied art of record, and are therefore in condition for allowance. Dependent claims 2-6 and 8-11 depend from the base claim 1 and introduce additional limitations therein. Likewise, dependent claims 17-19 and 21-24 depend from the base claim 16 and introduce additional limitations therein. Accordingly, these dependent claims are also believed to be allowable.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the present invention, as now defined by the independent claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present invention are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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